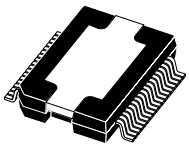
STA505

40V 3.5A QUAD POWER HALF BRIDGE

- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 200mΩ R_{dsON} COMPLEMENTARY DMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- THERMAL WARNING OUTPUT
- UNDER VOLTAGE PROTECTION

MULTIPOWER BCD TECHNOLOGY



PowerSO36

ORDERING NUMBER: STA505

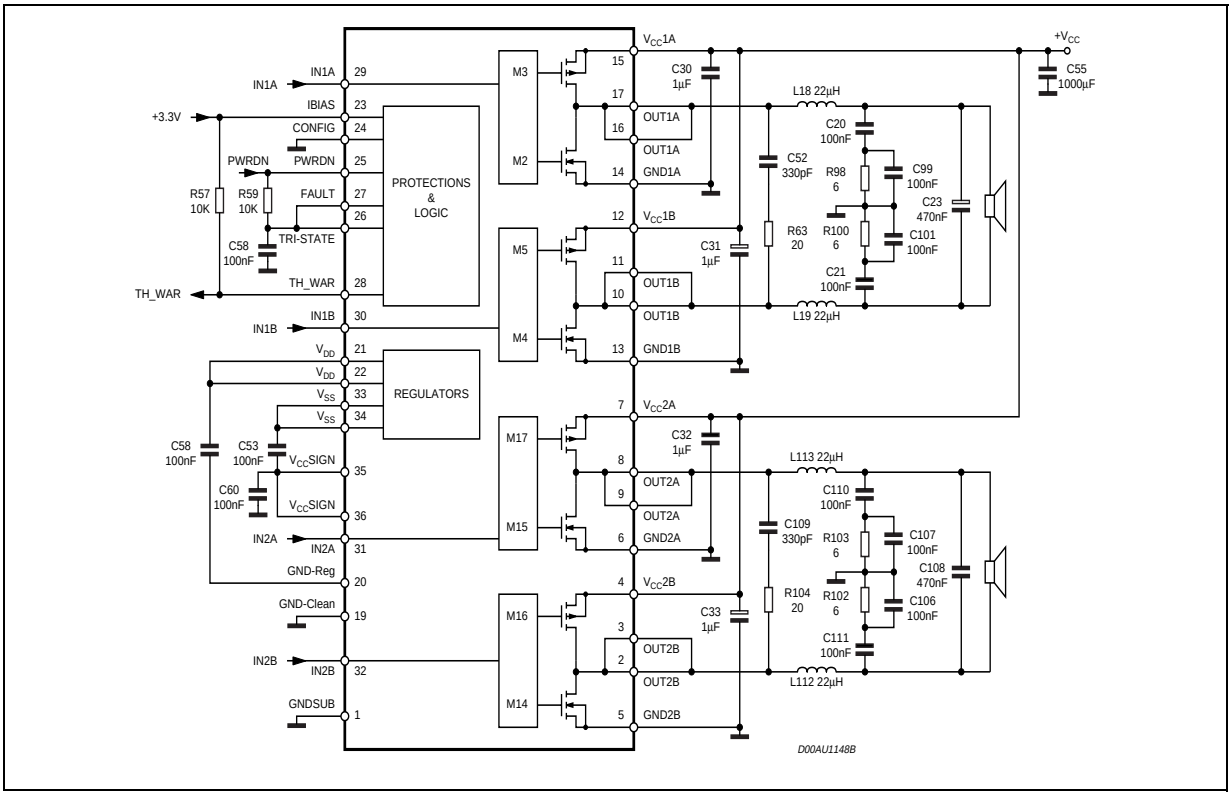
DESCRIPTION

STA505 is a monolithic quad half bridge stage in Multipower BCD Technology. The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to Vdd pin, as single bridge with double current capability.

The device is particularly designed to make the output stage of a stereo All-Digital High Efficiency (DDX™) amplifier capable to deliver 50 + 50W @ THD = 10% at V_{cc} 30V output power on 8Ω load and 80W @ THD = 10% at V_{cc} 36V on 8Ω load in single BTL configuration.

The input pins have threshold proportional to Ibias pin voltage.

AUDIO APPLICATION CIRCUIT



PIN FUNCTION

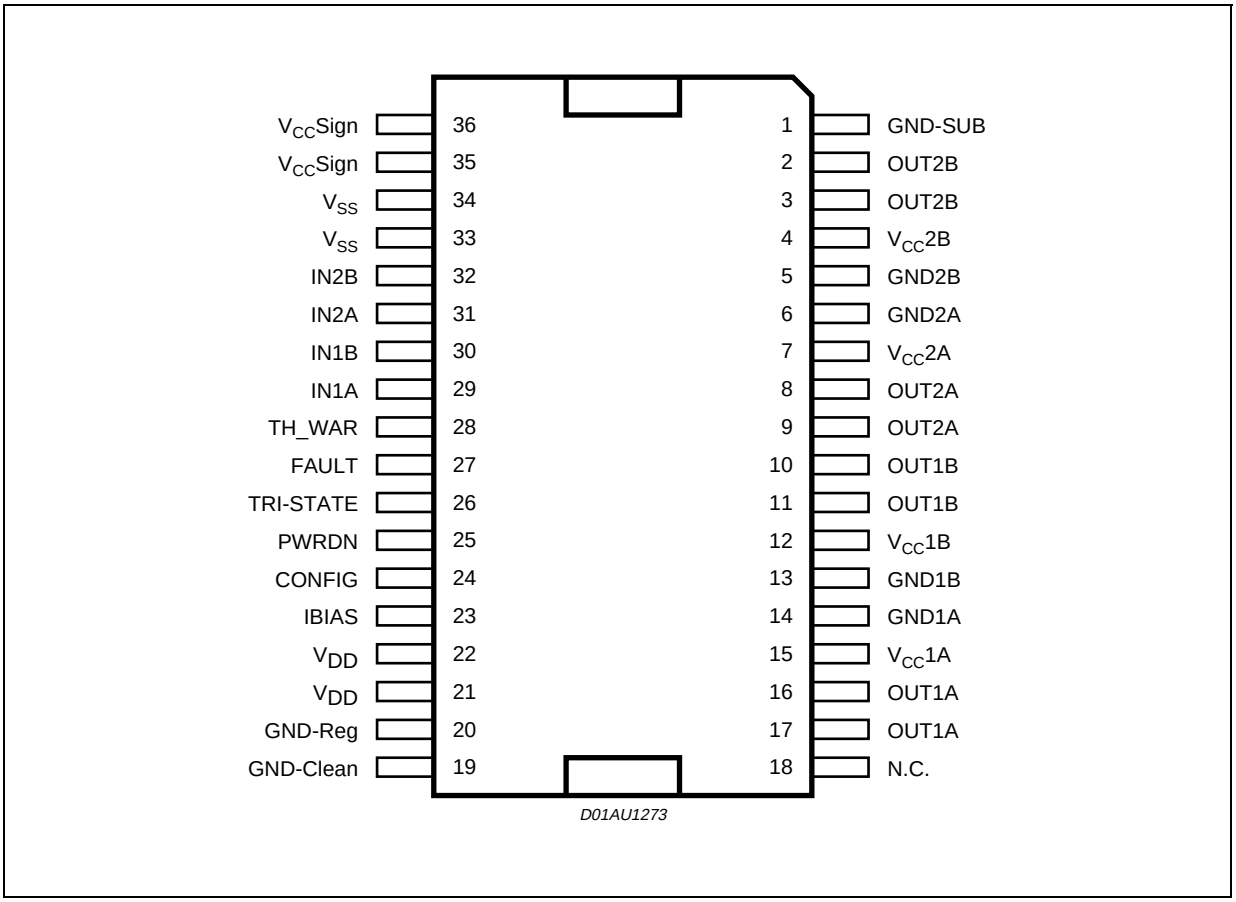
N°	Pin	Description
1	GND-SUB	Substrate ground
35 ; 36	Vcc Sign	Signal Positive supply
15	Vcc1A	Positive supply
12	Vcc1B	Positive supply
7	Vcc2A	Positive supply
4	Vcc2B	Positive supply
14	GND1A	Negative Supply
13	GND1B	Negative Supply
6	GND2A	Negative Supply
5	GND2B	Negative Supply
16 ; 17	OUT1A	Output half bridge 1A
10 ; 11	OUT1B	Output half bridge 1B
8 ; 9	OUT2A	Output half bridge 2A
2 ; 3	OUT2B	Output half bridge 2B
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
21 ; 22	Vdd	5V Regulator referred to ground
33 ; 34	Vss	5V Regulator referred to +Vcc
25	PWRDN	Stand-by pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
24	CONFIG	Configuration pin
28	TH-WAR	Thermal warning advisor
19	GND-clean	Logical ground
23	IBIAS	High logical state setting voltage
18	NC	Not connected
20	GND-Reg	Ground for regulator Vdd

FUNCTIONAL PIN STATUS

PIN NAME	Logical value	IC -STATUS
FAULT	0	Fault detected (Short circuit, or Thermal ..)
FAULT *	1	Normal Operation
TRI-STATE	0	All powers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorpion
PWRDN	1	Normal operation
THWAR	0	Temperature of the IC =130C
THWAR*	1	Normal operation
CONFIG	0	Normal Operation
CONFIG**	1	OUT1A=OUT1B ; OUT2A=OUT2B (IF IN1A = IN1B; IN2A = IN2B)

* : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.
**: To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd)

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CE}	DC Supply Voltage (Pin 4,7,12,15)	40	V
V_{max}	Maximum Voltage on pins 23 to 32	5.5	V
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

ELECTRICAL CHARACTERISTCS (Ibias = 3.3V; Vcc = 30V; T = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Power Pchannel/Nchannel MOSFET RdsON	Id=1A;T=25°C		200	270	mΩ
	Power Pchannel/Nchannel leakage Idss	Vcc=35v;T=25°C			50	µA
	Power Pchannel RdsON Matching	Id=1A; T=25°C	95			%
	Power Nchannel RdsON Matching	Id=1A; T=25°C	95			%
	Low current Dead Time (static)	see test circuit no.1; T=25°C; see fig. 1		10	20	ns
	High current Dead Time (dinamic)	L=22µH; C = 470nF; Rl = 8 Ω Id=3.5A; T=25°C; see fig. 3			50	ns
	Turn-on delay time	Resistive load; Vcc=30V;T=25°C			100	ns
	Turn-off delay time	Resistive load; Vcc=30V;T=25C			100	ns
	Rise time	Resistive load; as fig.1;T=25°C			25	ns
	Fall time	Resistive load; as fig. 1;T=25°C			25	ns
	Supply voltage operating voltage		10		36	V
	High level input voltage				Ibias/2 +300mV	V
	Low level input voltage		Ibias/2 -300mV			V
	Hi level Input current	Pin voltage=Ibias		1		µA
	Low level input current	Pin voltage = 0.3V		1		µA
	Hi level PWRDN pin input current	Ibias = 3.3V		35		µA
	Low logical state voltage VL (pin PWRDN, TRISTATE) (note 1)	Ibias = 3.3V	0.8			V
	High logical state voltage VH (pin PWRDN, TRISTATE) (note 1)	Ibias = 3.3V			1.7	V

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Supply current from Vcc in Power Down	PWRDN = 0			3	mA
	Output Current pins FAULT -TH-WARN when FAULT CONDITIONS	Vpin = 3.3V		1		mA
	Supply current from Vcc in Tri-state	Vcc=30V; Tri-state=0; T=25°C		22		mA
	Supply current from Vcc in operation (both channel switching)	Vcc=30V; Input pulse width = 50% Duty; Switching Frequency = 384Khz; No LC filters;		80		mA
	Isc (short circuit current limit) (note 2)	Vcc = 30V;T = 25°C	3.5	6	8	A
	Undervoltage protection threshold	T = 25°C		7		V
	Output minimum pulse width	No Load	70		150	ns

Notes: 1. The following table explains the VL, VH variation with Ibias

Ibias	VLmin	VHmax	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Note 2: If used in single BTL configuration, the device may be not short circuit protected

LOGIC TRUTH TABLE (see fig. 2)

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	OUTPUT MODE
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 1. Test Circuit.

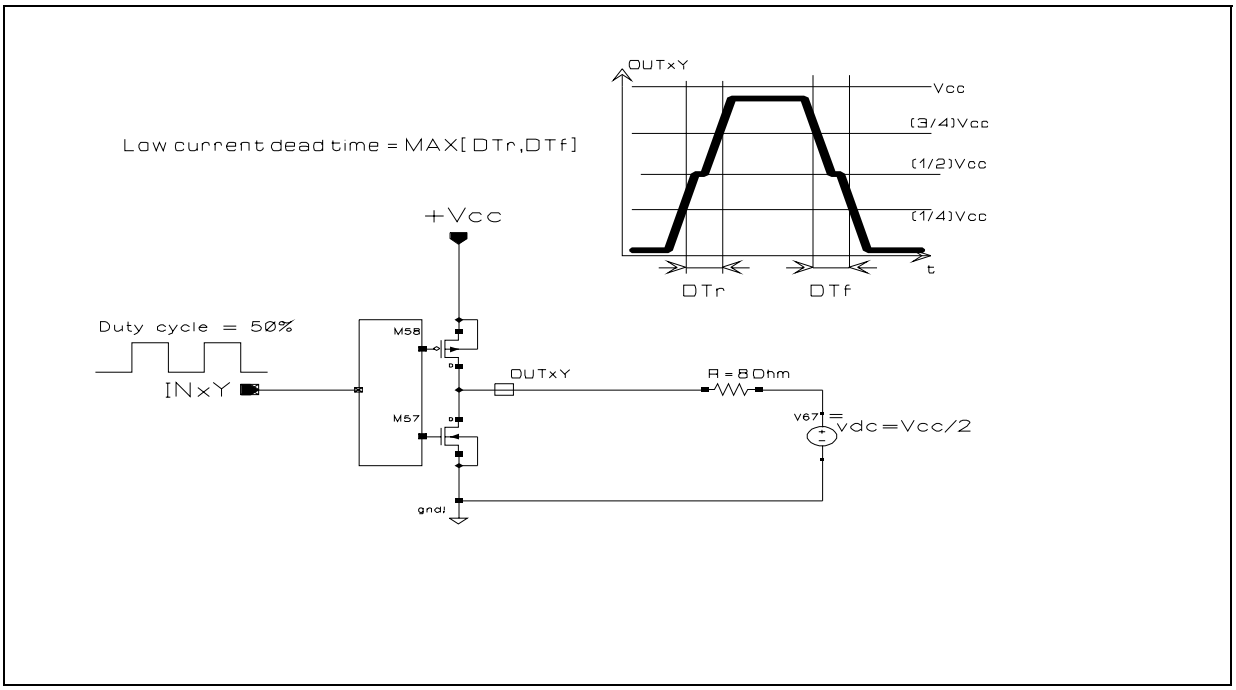


Figure 2.

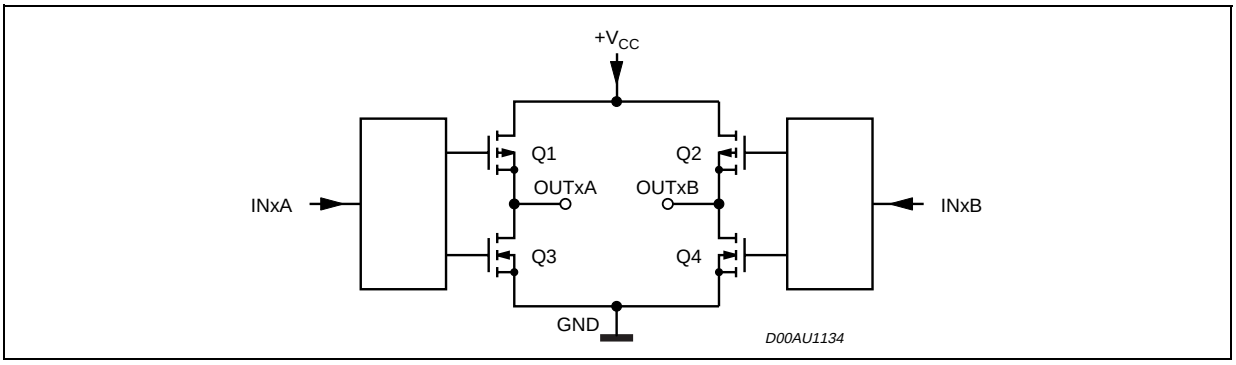


Figure 3.

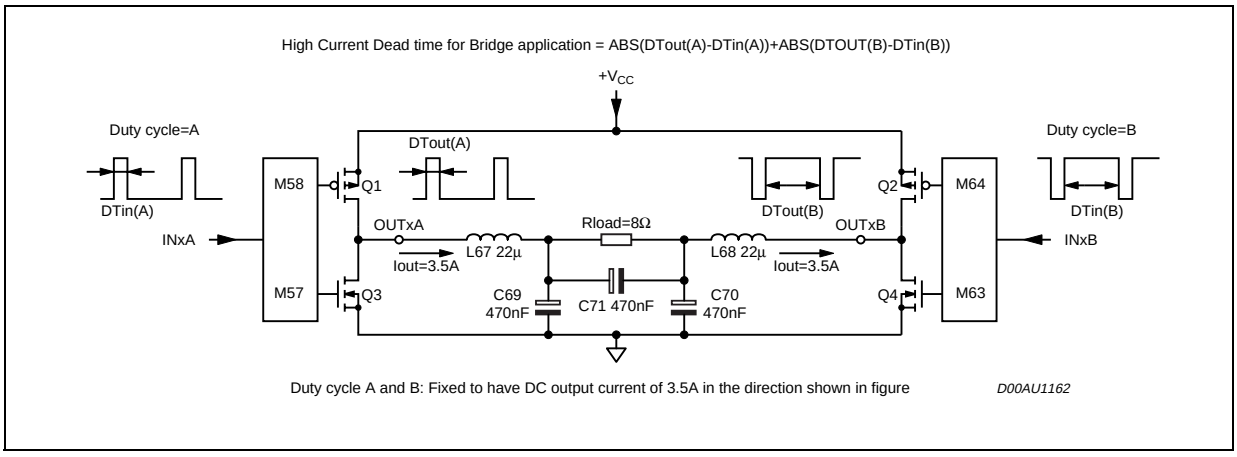
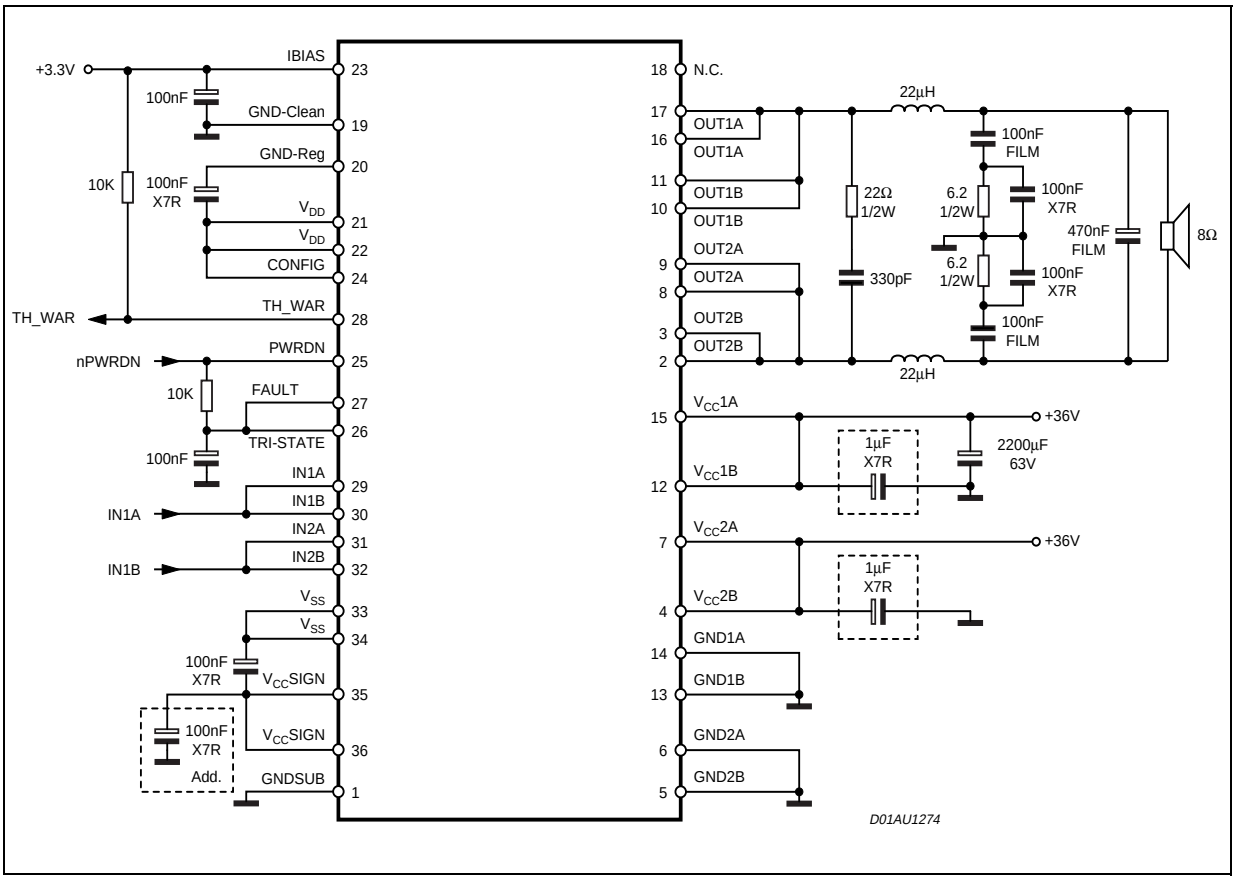


Figure 4. Typical Single BTL Configuration to obtain 80W @ THD 10%, R_L = 8Ω, V_{CC} = 36V (note 1)

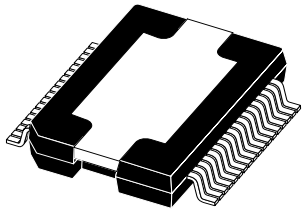


Note: 1. "A PWM modulator as driver is needed . In particular, this result is performed using the STA30X+STA50X demo board".

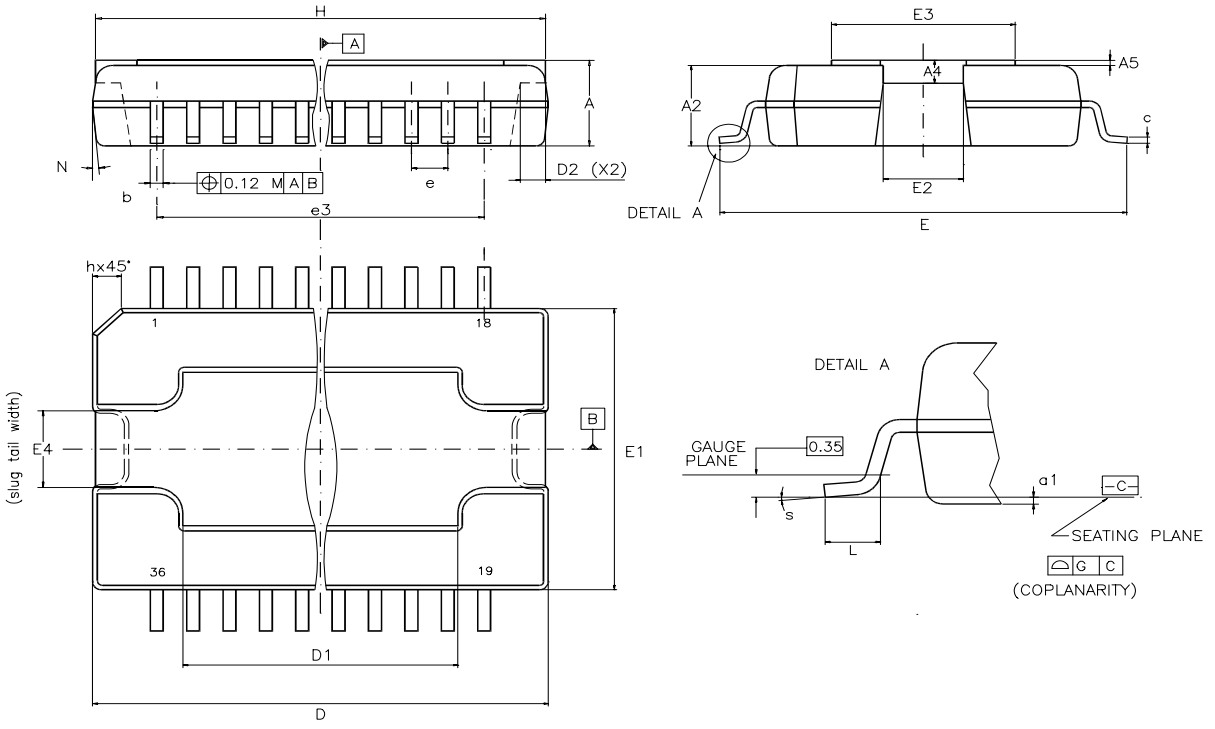
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.5	0.128		0.138
A2			3.3			0.13
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0		0.075	0		0.003
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max)					
s	8° (max)					

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.

OUTLINE AND MECHANICAL DATA



PowerSO36 (SLUG UP)



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